REMARKS

Claims 1-13 and 16-18 are pending in this application.

Reconsideration and review on the merits are respectfully requested.

Examiner's Interview

Applicants appreciate the Examiner's courtesy in granting the personal interview of March 31, 2003, with the undersigned. The Interview Summary prepared by the Examiner should correctly state that this was a personal interview. In the interview, Applicants' representative discussed a proposed amendment to claims 1, 2 and 4, relative to the applied prior art, to recite that the capacitor and the printed wiring substrate are fixed together with an insulating resin filling a gap between the cavity and the capacitor. No agreement was reached.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-13 and 16-18 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent 6,218,729 to Zavrel, Jr. et al. The grounds for rejection remain the same as set forth in the previous Office Action.

In response to the remarks portion of the Amendment Under 37 C.F.R. § 1.116 filed October 30, 2002, and referenced in the Request for Continuing Examination filed November 20, 2002, the Examiner maintained that Zavrel discloses an accommodation cavity defined by vias 850, 856 and the bottom layer 812, further asserting that this cavity is formed for the same

purpose as claimed in the present application, containing a capacitor in the substrate. The Examiner concludes that the presently claimed cavity is inherent in Zavrel.

Applicants respectfully traverse and request that the Examiner reconsider and withdraw the rejection for the following reasons.

First, Applicants amend Claims 1, 2 and 4 to more clearly state their claimed invention. Support for the fixing location of the insulating resin on the vertical sides of the capacitor wherein the vertical sides of the capacitor and the printed wiring substrate are fixed together with an insulating resin filling a gap between the cavity and the capacitor can be found, for example, at page 58, lines 9-13 and in Figs. 1 and 7(b). No new matter has been added, and entry of the amendment is hereby requested.

Applicants assert at least two distinctions over the cited reference to Zavrel. Specifically, Applicants point to a distinction between the "insulating resin" and the "insulating layer" in the prior art. The alternating "insulating layers" in Zavrel do not fix a built-in capacitor on which an IC chip is mounted. Rather, the insulating layers in Zavrel separate alternating metal layers and form the dielectric of the capacitor (col. 3, lines 1-26 of Zavrel). In the present invention, the "insulating resin" fixes together the vertical sides of the capacitor and the printed wiring substrate by filling a gap therebetween.

Applicants also point out that in Zavrel, there is no gap to be filled with an insulating resin because the cavity (in the Examiner's view) is the same size as the capacitor. However, in the present invention, the cavity and the vertical sides of the capacitor define a gap filled with an insulating resin.

As noted above, Applicants amend Claims 1, 2 and 4 to provide clarification on the location/position of the gap between the cavity and the capacitor and similar clarification on the location/position of the insulating resin filling the gap. The amended claims define the location of the insulating resin along the vertical sides of the capacitor and the printed wiring substrate in order to fix the two together.

Second, Applicants respectively submit that now the dispositive claim language patentably distinguishes over the applied prior art as previously asserted in the Amendment under 37 C.F.R. § 1.116 and incorporated herein by reference.

As required by the amended claims, the printed wiring substrate comprises a capacitor accommodation cavity for accommodating the capacitor wherein the vertical sides of the capacitor and the printed wiring substrate are fixed together with an insulating resin filling a gap between the cavity and the capacitor. Applicants continue to disagree with the Examiner in that capacitor plates 860 and 862 of Zavrel are embedded in the laminated substrate 822. Zavrel does not disclose a capacitor accommodation cavity, does not disclose a gap defined between the vertical sides of the capacitor and the printed wiring substrate, and does not disclose an insulating resin filling the gap with an insulating resin to fix together the vertical sides of the capacitor and the printed wiring substrate. Rather, as described by Zavrel, the substrate has a laminated structure of interconnects, where passive devices (such as capacitor 804) are designed into the metal interconnect layers (column 2, lines 2-8). Zavrel et al goes on to further describe the method of fabricating the substrate at column 2, lines 20-22. That is, the passive components including capacitor 804 in Zavrel are fashioned by selectively etching the metal interconnect

layers in the laminated structure. This is not a description of a capacitor accommodation cavity for receiving a capacitor which is fixed to the wiring substrate with an insulating resin. Rather, capacitor plates 860 and 862 in Zavrel are embedded in the laminated substrate.

Thus, Zavrel does not disclose a capacitor accommodation cavity wherein the vertical sides of the capacitor and the printed wiring substrate are fixed together with an insulating resin filling a gap between the cavity and the capacitor as required by the present claims.

The significance of the claimed capacitor accommodation cavity for accommodating the capacitor is discussed bridging pages 15-16 of the specification. Particularly, by employing the capacitor accommodation cavity, the capacitor terminals and the substrate terminals are densely located on and around the capacitor. Therefore, the planar size of the IC chip to be connected to the terminals can be made as small as possible, thereby preventing a problem in which the planar size cannot be reduced due to arrangement of the terminals.

For the above reasons, it is respectfully submitted that the present claims are patentable over Zavrel et al, and withdrawal of the foregoing rejections is respectfully requested. Withdrawal of all rejections and allowance of claims 1-13 and 16-18 is earnestly solicited.

In the event that the Examiner believes that it may be helpful to advance prosecution of this application, the Examiner is invited to contact the undersigned at the local Washington, D.C. telephone number indicated below.

Respectfully submitted,

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APPENDIX
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (Five times amended) A printed wiring substrate having a planar surface and a built-in capacitor having vertical sides on which an IC chip is mounted, said printed wiring substrate comprising a capacitor accommodation cavity selected from the group consisting of a closed-bottom cavity and a through hole cavity extending in the thickness direction of the printed wiring substrate and a capacitor disposed in said cavity, wherein the vertical sides of the capacitor and the printed wiring substrate are fixed together with an insulating resin filling a gap between the cavity and the capacitor, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

the capacitor comprises a plurality of capacitor terminals, wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode groups;

the printed wiring substrate comprises a plurality of substrate terminals;

the IC chip comprises a plurality of connection-to-capacitor terminals and a plurality of connection-to-substrate terminals;

the plurality of capacitor terminals of the capacitor are respectively flip-chip-bonded directly to a plurality of connection-to-capacitor terminals of the IC chip; and

the plurality of substrate terminals of the printed wiring substrate are respectively flip-chip-bonded to a plurality of connection-to-substrate terminals of the IC chip.

2. (Five times amended) A printed wiring substrate having a planar surface and a built-in capacitor having vertical sides on which an IC-chip-carrying printed wiring substrate is mounted, said printed wiring substrate comprising a capacitor accommodation cavity selected from the group consisting of a closed-bottom cavity and a through hole cavity extending in the thickness direction of the printed wiring substrate and a capacitor disposed in said cavity, wherein the vertical sides of the capacitor and the printed wiring substrate are fixed together with an insulating resin filling a gap between the cavity and the capacitor, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

the capacitor comprises a plurality of capacitor terminals, wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode groups;

the printed wiring substrate comprises a plurality of substrate terminals;

the IC chip-carrying printed wiring circuit comprises a plurality of connection-to-capacitor terminals and a plurality of connection-to-substrate terminals;

the plurality of capacitor terminals of the capacitor are respectively bonded in a connection-face-to-connection-face manner directly to a plurality of connection-to-capacitor terminals of the IC-chip-carrying printed wiring substrate; and

the plurality of substrate terminals of the printed wiring substrate are respectively bonded in a connection-face-to-connection-face manner to a plurality of connection-to-substrate terminals of the IC-chip-carrying printed wiring substrate.

4. (Four times amended) A printed wiring substrate having a planar surface and a built-in capacitor having vertical sides for mounting an IC chip or IC-chip-carrying printed wiring substrate having a plurality of connection-to-capacitor terminals and a plurality of connection-to-substrate terminals, said printed wiring substrate comprising a capacitor accommodation cavity selected from the group consisting of a closed-bottom cavity and a through hole cavity extending in the thickness direction of the printed wiring substrate and a capacitor disposed in said cavity, wherein the vertical sides of the capacitor and the printed wiring substrate are fixed together with an insulating resin filling a gap between the cavity and the capacitor, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

the capacitor comprises a plurality of capacitor terminals capable of being respectively flip-chip-bonded or bonded in a connection-face-to-connection-face manner to a plurality of connection-to-capacitor terminals of the IC chip or IC-chip-carrying printed wiring substrate, wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode group; and

the printed wiring substrate comprises a plurality of substrate terminals capable of being respectively flip-chip-bonded or bonded in a connection-face-to-connection-face manner directly

to a plurality of connection-to-substrate terminals of the IC chip or IC-chip-carrying printed wiring substrate.